REMARKS

The claims previously in the case have been replaced by a set of new claims that are believed to be proper as to form and clearly patentable over the cited references.

Reconsideration is accordingly respectfully requested, for the rejection of the claims as anticipated by, or unpatentable over VAN HOOF et al., alone or in view of the article by WALLACE et al.

VAN HOOF discloses contexts processed in a pipelined manner, the contexts passing a plurality of consecutive stages. VAN HOOF also discloses, (see e.g. Fig. 7). executing an initial step, (e.g. an instruction fetch), of a first operation on a context, and subsequently commencing an execution on the context of an initial step, (e.g. an instruction fetch), of a second operation before completing an execution on the context of a following step, (e.g. instruction decoding), of the first operation. More particularly, the initial step of the second operation and the following step of the first operation are carried out in the same clock cycle.

However, VAN HOOF suggests receiving at one stage a plurality of contexts, and performing in each stage all steps of entire operations on each context. Thereby, the sub-processor of the stage needs to alternate between processing of different contexts, handle potential stalls, and allow contexts to pass each other, (see e.g. column 2, lines 18-60). This in turn

requires arrangements for intermittent storage of contexts depending on results of operation steps, and scheduling of contexts between the processing stages. Such conditional storage and conditional relocations of contexts requires hardware and logic in addition to what is needed for the direct operations on the context data, (e.g. fetch, decode, etc.). and it will also add to the time of the overall processing of the contexts.

By contrast, the object of the present invention is to increase the rate of data being processed. This object is reached, as defined in new claim 10, by receiving, at each clock cycle of the processor, the context at one of the stages from the preceding stage, executing the initial step of the first operation on the context at a first stage, executing the following step of the first operation on the context at a second stage, and executing the initial step of the second operation on the context at a second stage.

Thus, in sharp contrast with VAN HOOF, the present invention provides for, at each clock cycle, unconditionally moving the context to the next stage of the pipeline, and performing the steps of each operation on the context in separate stages. This is done in combination with performing the steps of separate operations on the context in the same stage.

This provides the advantage of increasing the data processing rate, by combining pipelining of contexts with pipelining operations on each context. As opposed to Van Hoof,

this advantage is provided without the need for any hardware or logic for intermittent storage of contexts depending on results of operation steps, and scheduling of contexts between the processing stages.

Instead of giving any hint towards the present solution, VAN HOOF emphasizes the concurrent operations on a plurality of contexts at each stage giving said conditional storage and relocations.

The article by WALLACE et al. may teach the feature for which it was cited; but as WALLACE et al. does nothing to overcome the fundamental deficiencies of VAN HOOF, pointed out above, it is not believed to be necessary to discuss WALLACE et al. in greater detail at this time.

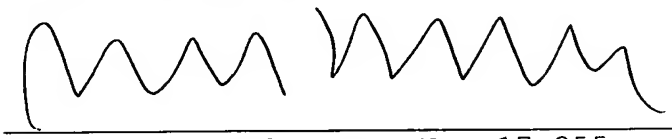
As the claims now in the case bring out these distinctions with ample particularity, it is believed that they are all patentable, and reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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